Amendments to the Claims:
This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:
Claim 1 (canceled)

Claim 2 (currently amended): ~~The system of claim 1,~~ A system comprising:

a first logic circuit configured to receive one or more logic circuit input signals and to generate a logic circuit output signal; and

a multiplexer configured to receive the logic circuit output signal and one or more additional signals as multiplexer input signals, wherein the multiplexer is configured to receive a select signal that controls the multiplexer to select one of the multiplexer input signals to be provided as a multiplexer output signal;

wherein when the select signal controls the multiplexer to select the logic circuit output signal as the multiplexer output signal, the first circuit operates in a first mode, and when the select signal controls the multiplexer to deselect the logic circuit output signal as the multiplexer output signal, the first circuit operates in a second mode wherein the second mode comprises a power-saving mode.

Claim 3 (currently amended): The system of claim 2~~1~~, wherein when the first logic circuit operates in the second mode, the logic circuit output signal contains fewer data transitions than when the first logic circuit operates in the first mode.

Claim 4 (original): The system of claim 3, wherein when the first logic circuit operates in the second mode, the logic circuit output signal contains no data transitions.

Claim 5 (currently amended): The system of claim 2~~1~~, wherein the first logic circuit operates according to a first truth table in the first mode and according to a second truth table in the second mode, and wherein the first truth table is not identical to the second truth table.

Claim 6 (currently amended): The system of claim 2~~1~~, wherein the first logic circuit functions as an XOR gate in the first mode.

Claim 7 (currently amended): The system of claim 2~~1~~, wherein the first logic circuit functions as an XNOR gate in the first mode.

Claim 8 (original): The system of claim 7, wherein the multiplexer is configured to invert the logic circuit output signal when the first logic circuit is selected.

Claim 9 (currently amended): The system of claim 2~~1~~, wherein the multiplexer is configured to receive only 2 multiplexer input signals.

Claim 10 (currently amended) The system of claim 2~~1~~, wherein the multiplexer is configured to receive more than 2 multiplexer input signals.

Claim 11 (canceled)

Claim 12 (currently amended) ~~The method of claim 11,~~ A method comprising:

providing a first logic circuit configured to receive one or more logic circuit input signals and to generate a logic circuit output signal;

providing a multiplexer configured to receive the logic circuit output signal and one or more additional signals as multiplexer input signals, wherein the multiplexer is configured to receive a select signal that controls the multiplexer to select one of the multiplexer input signals to be provided as a multiplexer output signal; and

operating the first logic circuit in a first mode when the first logic circuit is selected by the multiplexer and operating the first logic circuit in a second mode when the first logic circuit is deselected by the multiplexer, wherein the operation of the

first logic circuit is different in the first and second modes wherein the second mode comprises a power-saving mode.

Claim 13 (currently amended): The method of claim 12~~11~~, further comprising reducing data transitions in the first logic circuit in the second mode, as compared to the first mode.

Claim 14 (original): The method of claim 13, further comprising eliminating data transitions in the first logic circuit in the second mode.

Claim 15 (currently amended): The method of claim 12~~11~~, operating the first logic circuit according to a first truth table in the first mode and according to a second truth table in the second mode, wherein the first truth table is not identical to the second truth table.

Claim 16 (currently amended): The method of claim 12~~11~~, operating the first logic circuit as an XOR gate in the first mode.

Claim 17 (currently amended): The method of claim 12~~11~~, operating the first logic circuit as an XNOR gate in the first mode.

Claim 18 (original): The method of claim 17, inverting the logic circuit output signal when the first logic circuit is selected.

Claim 19 (currently amended): The method of claim 12~~11~~, controlling the multiplexer to select from only 2 multiplexer input signals.

Claim 20 (currently amended): The method of claim 12~~11~~, controlling the multiplexer to select from more than 2 multiplexer input signals.